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Systems

Agile Coherent Synthesizer (ACS)
Summary Technical Specifications

ACS-25018
ACS-85018

Version 1.3

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Summary Technical Specifications

1 INTRODUCTION

This document specifies the technical requirements for the ACS-25018 and ACS-85018 agile coherent synthesizers. The synthesizer unit is a coherent phase, frequency-agile instrument that generates signals over a wide frequency range.

2 FREQUENCY

2.1.1 Frequency Bands

The ACS synthesizer covers the frequency bands listed below.

Frequency	Coverage Per Unit:
UHF	250-1050 MHz (Output #1, ACS-25018 only)
L-Band through Ku -Band	850-18000 MHz (Output #2)

2.1.2 Frequency Resolution

Minimum frequency step size:	<1 Hz

2.1.3 Frequency Agility

Agile Bandwidth:	Entire band of coverage at each output port
Switching Speed:	< 1 usec, 300 nsec typ
Settling:	< 1 degree of the final phase < 0.1 dB of the final amplitude

2.1.4 Phase Coherency

Phase coherent frequency switching is the ability of the synthesizer to change frequency arbitrarily and when the original frequency is revisited, the phase relationship between the synthesizer and a stationary reference remains the same. Frequency switching shall be phase coherent at any output frequency or step size.

3 SPECTRAL PURITY

Spurious: <-60 dBc for output power of +10 dBm
Harmonics <-30 dBc for output power of +10 dBm
Phase Noise:

Offset from Carrier	Typ SSB Phase Noise (dBc/Hz) 0.25-18 GHz
1 Hz *	-30
10 Hz *	-55
100 Hz	-80
1 KHz	-90
10 KHz	-100
100 KHz	-110
1 MHz	-130
10 MHz	-140

* Internal Reference Mode Only

AM Noise floor: -125 dBm/Hz typ for output power of +10 dBm

4 FREQUENCY REFERENCE

The synthesizer has the capability to automatically select internal or external reference mode.

4.1 Internal Reference Oscillator

Frequency: 10 MHz
Aging: $<5x10^{-10}$/day
Temperature Stability: $<1x10^{-8}$, 0 to 50 deg C (unlocked)
Output Amplitude: 0 dBm nominal at rear panel
Impedance: 50 ohms

4.2 External Reference Oscillator

Frequency: 10 MHz
Input Amplitude: 0 dBm $\pm$3 dB
Impedance: 50 ohms

5 AMPLITUDE

5.1 Output Power

Output Power: +10 dBm into a 50 ohm load
Output power programmable from 0-10 dBm in 0.5 dB steps for any programmed frequency

5.2 Flatness

Amplitude Flatness:	± 1.5 dB flatness over entire band

5.3 Accuracy

Amplitude Accuracy:	± 1.5 dB of the specified output power level

5.4 Stability

Amplitude Stability:	<0.2 dB amplitude variation at same commanded frequency over 1 minute

5.5 Programmable Fast level Attenuation

Dynamic Range:	>10 dB
Resolution:	0.5 dB
Switching:	< 1 us, 300 nsec typ.
Settling:	< 0.1 dB of final amplitude

5.6 Amplitude Calibration

The synthesizer performs internal automatic amplitude calibration over the full frequency range.

6 TIMING & CONTROL

6.1 System Configuration and Status

The synthesizer has a LAN interface for downloading waveform parameters to memory, entering system configuration and calibration data, verifying system status, and error reporting. A TCP/IP Internet protocol with text-based messaging is used for network communications. External devices connected to the synthesizer act as a controller by initiating all network communications. The synthesizer responds to all commands by returning the command status or requested parameters.

6.1.1 User Interface Software

A graphical user interface (GUI) is provided for configuration and monitoring of the ACS. The user interface software is a stand-alone executable capable of running under Windows XP operating systems.

6.1.2 Waveform Configuration

The system configuration interface allows the user to define waveform segments and sequences. Waveform segments consist of control parameters for frequency, amplitude, and dwell time. A waveform sequence specifies the order and timing control for synthesis of waveform segments.

The configuration inputs for waveform segments supports definition of the following parameters:

- Segment duration (dwell time)
- Carrier frequency
- Fast Level Attenuation (amplitude)

A waveform address is generated by the synthesizer configuration interface for each waveform segment defined by the user. Storage is provided to configure up to 65K segments with optional expansion to 256K segments.

Sequence control is configurable as internal or external mode. When set to internal sequencing mode, the order of waveform segments is determined by the configured sequence. In external mode the waveform segment address and trigger is controlled through an external interface.

Configuration of timing and control allows for enabling or disabling of external triggers. Enabling of a segment or sequence trigger shall cause the sequencer to advance when a trigger pulse is received. When triggers are disabled, the sequencer will automatically advance at the completion of a segment or sequence.

6.2 Waveform Address and Trigger

Waveform address and trigger control signals provide for real-time selection/addressing of configured waveform segments. The physical interface of the waveform address and trigger signals is selectable as either a serial fiber channel or a “copper” interface consisting of a TTL parallel port connection.

The optional fiber optic interface allows random access to the programmed waveform table by receiving a 3-byte address followed by 1 or more sync bytes. Changes in the 3-byte address act as a strobe, triggering the synthesizer to advance to the waveform segment stored at that address. 8b/10b encoding is used as defined in the Fibre Channel specification. The sync byte is the K28.5 Fibre Channel special character. Multiple sync bytes are used to allow the start of the sequence to be positioned with a time resolution of 1 byte.

The copper interface supports 16 parallel lines for addressing (65K waveform length limit), and 1 control line for triggering. The trigger pulse causes the synthesizer to latch the address from an external port and synthesize the waveform segment corresponding to the loaded address.

6.3 Waveform Sequence Trigger

The synthesizer interface includes an external TTL control signal interface to set the waveform address pointer to the beginning of the waveform sequence.

6.4 Waveform Segment Trigger

The synthesizer interface includes an external TTL control signal interface to advance the waveform address pointer to the next defined segment.

6.5 Waveform Markers

Two definable output timing pulses are provided that synchronous with the generation of each waveform segment or sequence.

6.6 Trigger Synchronization

The maximum delay from an external waveform trigger to the generation of the selected waveform does not exceed 1 usec.

The time jitter for an external waveform trigger and the generation of the selected waveform does not vary by more than ±10 nsec.

7 ELECTRICAL INTERFACE

RF Output:	Connector: Precision N Type Female Impedance: 50 ohms Multiple outputs as denoted in section 2.1.1 Max VSWR: <2.0:1 Max Reverse Power: + 20 dBm Panel location: Front Panel
System Configuration & Status:	Connector: RJ45 Physical Interface: Ethernet 10/100BASE-T
Waveform Address/Trigger Control Copper:	Connector: 37 pin D connector Electrical Interface: TTL
Waveform Address/Trigger Control Fiber:	Connector: Duplex SC Physical Interface: Multimode Fiber
Waveform Segment Trigger:	Connector: BNC Female Electrical Interface: TTL, 50-ohm impedance
Waveform Sequence Trigger:	Connector: BNC Female Electrical Interface: TTL, 50-ohm impedance
Waveform Segment Marker:	Connector: BNC Female Electrical Interface: TTL, 50-ohm impedance
Internal 10 MHz Reference:	Connector: BNC Female Electrical Interface: 50-ohm impedance
External 10 MHz Reference:	Connector: BNC Female Electrical Interface: 50-ohm impedance
Serial Debug Messaging:	RS-232, 9-pin D
Line-ON/OFF Switch:	Toggle Control
AC Power:	3 pin AC connector for primary power 100-240 VAC, 50/60 Hz

8 BUILT-IN-TEST

System built-in-test includes but is not limited to the following:

- Error reporting with timestamp via Ethernet
- Panel display for alert of hardware problems
- Verify lock status of 10/100 MHz PLXOs
- Verify LRU output signal levels
- External reference detection and lock status
- Internal reference detection and lock status
- Verify power supply voltage levels are within acceptable levels

9 GENERAL REQUIREMENTS

9.1 Operating Temperature

Temperature Range:	5 deg C to 35 deg C

9.2 Electromagnetic Compatibility

The synthesizer is designed and constructed for suppression of electromagnetic disturbances. The following guidelines are followed to prevent degradation of performance in the presence of conducted or radiated energy:

- All openings (including cooling/ventilation openings) are provided with RF absorbing filters or screens
- All removable joints are provided with RF gaskets.

9.3 Power Requirements

Power:	100 to 240 VAC, 50/60 Hz, 200 watts max.

9.4 Physical Dimensions

Size:	Standard 19 inch rack mountable unit, 3U high, maximum depth 27”
Weight:	23 kg